REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 15 November 2006. Responsive to the rejections made in the Official Action, Independent Claims 6 and 12 have been amended to further emphasize the distinguishing features of the present invention over the cited prior art. Claims 1 – 5 have been canceled without prejudice or disclaimer of the subject matter thereof. Claims 10 – 11, 16 and 20 have been canceled without prejudice to incorporate the subject matter thereof in their respective base claims.

In the Official Action, Claims 1 – 3, 12 – 15, and 17 – 19 were rejected under 35 U.S.C. § 102(b) as being unpatentable by Yuen, U.S. Patent 5,357,628; Claims 4 – 11 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yuen in view of Dunlap, U.S. Patent 6,615,368; and Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yuen in view of Klein, U.S. Patent Application Publication 2001/0016892 A1.

Yuen, the primary reference cited by the Examiner, is directed to debugging of a computer system which includes a CPU 12, a chip input/output unit GENIO, and a single chip graphics interface GENVGA. The CPU 12 comprises debug read/write registers and debug I/O ports for interfacing with debugging functions disposed on logic external to the CPU for debugging the computer system. Additionally, CPU 12 comprises logic for executing a plurality of hardware interrupt. Interrupts are serviced after execution of the current instruction. After

the interrupt service routine is finished, execution proceeds with the instruction immediately after an interrupted instruction.

A system management mode (SMM) is provided to the computer system in the Yuen reference system so that debugging and various other system management functions are performed under SMM. A system management interrupt (SMI) is provided to put the computer system into SMM. A SMI handler having an integrated debugger is provided to service the SMI. The SMI handler determines the SMI triggering event and performs the system management functions accordingly, invoking its integrated system management function handlers such as the integrated debugger if necessary.

The integrated debugger provides debugging functions such as displaying register contents, displaying memory contents, displaying interrupt vector locations, displaying BIOS data areas, editing register and/or memory contents, establishing break points for I/O and memory accesses, single stepping execution. A resume instruction (RSM) is provided for returning the computer system to the state just before the SMI was detected and resuming execution at the next instruction of the interrupted program. Various mechanisms are provided for triggering a SMI, such as for example, external SMI pin, software SMI event trap, local and global timers.

It is respectfully submitted that Yuen, in contrast to the present invention, is silent as to using a pop-up debugging operation window when the CPU 12 has

entered a system management mode.

Opposingly in the present invention, the debugging program is executed to pop-up or debugging operation window upon the CPU having entered a system management mode. In the present invention, each debugging item to be executed is selected in the debugging operation window. Further, in the present invention, a user sets a trap address for the debugging operation window, so that after leaving the debugging operation window upon the execution of the debugging item, the debugging operation window pops up repeatedly from the set trap address each time the CPU enters the system management mode. This feature is completely missing in Yuen.

Further, in Yuen, the chips GENIO and GENVGA are not presented as South-bridge chipset and/or North-bridge chipset.

While in the present invention, the CPU is connected to a North-bridge chipset and a South-bridge chipset, as shown in Figure 1, so that upon triggering of the South-bridge chipset, the system management interrupt signal is sent therefrom to the CPU. This feature additionally is not shown in Yuen.

Dunlap, another reference cited by the Examiner is directed to debugging highly integrated data processors. The system includes a CPU 105 which is connected to a chipset bridge 155. The data processor 100 has debugging features that output from the data processor 100 selected instructions, data, or addresses in response to the occurrence of one or more of events in the data processor. These

events include execution of a branch instruction, detection of a trigger value on an internal bus, or execution of a unique spray instruction. The debugging apparatus is capable of detecting a trigger, such as execution of spray operational code that sets a spray flag, execution of an operational code that has a parity debug bit set, and a debug match set by a debug registers that sets a spray flag. In response to the detection of the trigger, the debugging apparatus initiates an operation of the programmable logic analyzer and initiates a debug system management interrupt routine.

It is respectfully submitted, that in Dunlap, no explicit disclosure of a pop out debugging operation window is presented. The Examiner made an assertion that the reference suggests in column 1, lines 39 – 45 to pop out a debugging operation window after the central processing unit entered a system management mode.

It is respectfully submitted that, as expressed in column 1, lines 39 – 45 of Dunlap, "... a debugger ... causes a program to execute to some break point and then halt. This allows a programmer to modify a memory, to analyze certain registers (such as debug registers) that are accessible in the microprocessor, and to change breakpoints if necessary. Program execution may then be resumed."

Although suggesting some kind of interaction between a programmer and the debugging system, this reference, in contrast to the present invention, however fails to teach executing of the debugging program to pop out a debugging

operation window upon the CPU has entered a system management mode, and setting a trap address for said debugging operation window so that after leaving the debugging operation window after the execution of the debugging item has been accomplished, the debugging operation window is popped out from the pre-set trap address each time when the CPU enters the system management mode.

This feature of the debugging system and method of the present invention is completely missing in Dunlap.

Further, the chipset 155 of Figure 1 of Dunlap is not being presented as a South-bridge chipset and/or North-bridge chipset.

While in the present invention, the debugging system includes a North-bridge chipset and a South-bridge chipset both connected to the central processing unit, wherein the system management interrupt signal is sent from the South-bridge chipset to the central processing unit.

Klein, a further reference cited by the Examiner, is directed to a computer system for processing system management interrupt requests. This reference represents a South-bridge 34 and North-bridge 24 used in system management interrupt procedure.

However, in contrast to the present invention, Klein patent is silent on execution of debugging as it is focused on implementing control features, such as power management during the interrupt periods.

Further, the Klein reference fails to teach a debugging operation window

which is popped out after the central processing unit enters a system management mode, wherein a trap address for the debugging operation window is set, and wherein the debugging operation window is popped out repeatedly from the set trap address each time when the CPU enters the system management mode. This feature of the present invention is completely missing in the Klein patent.

It is respectfully submitted, that the references cited by the Examiner, taken singly or in combination, fail to teach a method or a device for debugging in a computer system in which a debugging tool program is executed to pop out a debugging operation window upon the CPU enters a system management mode, and wherein a trap address is set for the debugging operation window so that the debugging operation window is popped out repeatedly from the pre-set trap address each time when the South-bridge chipset is triggered.

Claim 6 has been amended to include (inter alia) the following limitations:

"... executing said debugging tool program to pop out a debugging operation window upon said central processing unit has entered a system management mode ...

... setting a trap address for said debugging operation window ...

... after leaving said debugging operation window upon the execution of said at least one debugging item has been accomplished, said debugging operation window is popped out repeatedly from said trap address each time when said South-bridge chipset is triggered...".

Claim 12 has been amended to include (inter alia) the following recitations:

"... a debugging operation window having a predetermined trap address...

... a unit retrieving said debugging operation window from said predetermined trap address each time said general purpose input/output pins of said South-bridge chipset are triggered".

Since the prior art references cited by the Examiner fail to teach each and every limitation of the present invention, as now claimed, none of them are believed to anticipate the claimed present invention. Additionally, since the prior art references, taken solely or in any combination thereof, fail to teach the combination of elements for the purposes and objectives as previously described, as claimed in each of Claims 1 and 6, the present invention is not believed to be obvious in view of the cited prior art.

Accordingly, Independent Claims 6 and 12, as amended, are believed to have patentable distinctions over the cited prior art; and the allowance of Claims 6 and 12, as amended, is respectfully requested.

Claims 7 – 9, dependent upon Claim 6, and Claims 13 – 15 and 17 – 19 dependent upon Claim 12, are each believed to add further patentable limitations in addition to be dependent upon the allowable base claims. Accordingly, the allowance of Claims 7 – 9, 13 – 15, and 17 – 19, is respectfully solicited.

It is believed that now the present Application is placed in condition for allowance and the same action is respectfully requested.

Best regards,
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